

REMARKS

In the Office Action mailed July 30, 2003, the Examiner rejected all of the pending claims citing U.S. Patent Nos. 5,396,170 (D'Souza et al.) and 6,411,116 (DeHaven et al.).

Claim 1 specifically claims that the DRAM dies are arranged in rows, that each row comprises a plurality of DRAM dies, that each DRAM die in a given row is daisy chained to the next DRAM die in the row, that the last DRAM die in a row is daisy chained to the first DRAM die in the next row via a metal line on a scribe area of the wafer, and that the DRAM dies on the wafer are connected to power busses along a scribe area so that the dies can be powered. Neither one of the cited references discloses or suggests providing such structure.

For example, D'Souza et al. '170 does not disclose providing the DRAMS in rows, or daisy chaining each of the rows as specifically claimed (i.e., that the last DRAM die in a row is daisy chained to the first DRAM die in the next row via a metal line on a scribe area of the wafer). Such arrangement and daisy-chaining provides for an efficient use of wafer real estate. It does not appear that D'Souza et al. '170 discloses DRAM dies arranged in rows on a wafer and connected to power busses along a scribe area of the wafer.

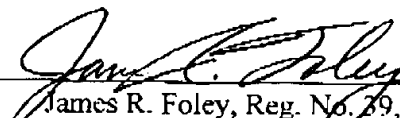
Serial No.: 09/918,183
Art Unit: 2829
Page 4

Applicant respectfully submits that the claims are allowable over the prior art of record, and respectfully requests that the application be passed to issuance.

Respectfully submitted,

Date: September 23, 2003

By


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Serial No.: 09/918,183

Art Unit: 2829

Page 5